IN THE CLAIMS:

Claims 1-25 have been amended herein. All of the pending claims 1 through 25 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Currently Amended) A method of assembling a flip-chip semiconductor device assembly, the method comprising:

providing a wafer having an active surface and a back surface and including a plurality of unsingulated semiconductor dice, at least some semiconductor dice of ~~said~~ the plurality having conductive bumps protruding transversely from ~~said~~ the active surface;

providing a wafer scale interposer substrate having a first surface and a second surface, ~~said~~ the wafer scale interposer substrate including a plurality of unsingulated interposer substrates, each having a plurality of conductive elements thereon adjacent ~~said~~ the second surface, each unsingulated interposer substrate dimensioned and located to correspond with one of ~~said~~ the plurality of semiconductor dice of ~~said~~ the wafer, each of ~~said~~ the plurality of interposer substrates having a plurality of recesses extending thereinto from ~~said~~ the first surface to expose at least a portion of one of ~~said~~ the plurality of conductive elements; and

placing ~~said~~ the wafer with ~~said~~ the active surface thereof facing ~~said~~ the first surface of ~~said~~ the wafer scale interposer substrate and ~~said~~ the plurality of unsingulated semiconductor dice in alignment with ~~said~~ the plurality of unsingulated interposer substrates and disposing each of ~~said~~ the conductive bumps protruding transversely from ~~said~~ the active surface into a recess of ~~said~~ the plurality of recesses of ~~said~~ the plurality of interposer substrates so that ~~said~~ the conductive bumps are substantially received within ~~said~~ the plurality of recesses in ~~said~~ the plurality of interposer substrates.

2. (Currently Amended) The method of claim 1, further comprising attaching ~~said~~ the active surface of ~~said~~ the wafer directly to ~~said~~ the first surface of ~~said~~ the wafer scale interposer substrate by at least one adhesive element disposed on ~~said~~ the first surface at a location of each of ~~said~~ the plurality of interposer substrates.

3. (Currently Amended) The method of claim 1, wherein ~~said~~ disposing comprises abutting ~~said~~ the active surface of ~~said~~ the wafer with ~~said~~ the first surface of ~~said~~ the wafer scale interposer substrate.

4. (Currently Amended) The method of claim 1, further comprising aligning each of ~~said~~ the conductive bumps on ~~said~~ the at least some semiconductor dice with ~~said~~ the plurality of recesses so that each of ~~said~~ the conductive bumps is positioned directly over one of ~~said~~ the plurality of recesses.

5. (Currently Amended) The method of claim 1, wherein ~~said~~ providing ~~said~~ the wafer scale interposer substrate comprises forming ~~said~~ the plurality of recesses to be sized and configured to substantially receive ~~said~~ the conductive bumps therein.

6. (Currently Amended) The method of claim 1, wherein ~~said~~ providing ~~said~~ the wafer scale interposer substrate comprises forming ~~said~~ the plurality of recesses collectively in each of ~~said~~ the semiconductor dice in at least one of a centrally aligned row configuration, a peripheral configuration and an I-shaped configuration.

7. (Currently Amended) The method of claim 1, wherein ~~said~~ disposing comprises positioning ~~said~~ the conductive bumps of ~~said~~ the plurality of semiconductor dice in ~~said~~ the recesses of ~~said~~ the plurality of an interposer substrate so that a surface of each of ~~said~~ the conductive bumps directly contacts a respective conductive element of the plurality of conductive elements.

8. (Currently Amended) The method of claim 1, further comprising bonding ~~each of said~~ the conductive bumps to ~~a said~~ the plurality of conductive ~~element.~~ elements, respectively.

9. (Currently Amended) The method of claim 8, wherein ~~said~~ bonding comprises bonding by at least one of reflowing, curing, ultrasonic bonding and thermal compression bonding.

10. (Currently Amended) The method of claim 1, further comprising disposing a nonsolid conductive material on ~~said~~ the conductive bumps prior to disposing ~~said~~ the conductive bumps in ~~said~~ the plurality of recesses.

11. (Currently Amended) The method of claim 10, further comprising bonding each of ~~said~~ the conductive bumps having ~~said~~ the nonsolid conductive material thereon to ~~a said~~ each of the plurality of conductive ~~element~~ elements using ~~said~~ the nonsolid material.

12. (Currently Amended) The method of claim 1, further comprising disposing a nonsolid conductive material in each of ~~said~~ the plurality of recesses.

13. (Currently Amended) The method of claim 12, wherein ~~said~~ disposing ~~said~~ the nonsolid conductive material comprises:

providing a stencil having a pattern of apertures therethrough corresponding to a pattern of ~~said~~ the plurality of recesses of ~~said~~ the plurality of unsingulated interposer substrates of ~~said~~ the wafer scale interposer substrate;

positioning ~~said~~ the stencil over ~~said~~ the wafer scale interposer substrate so that ~~said~~ the pattern of apertures corresponds with ~~said~~ the pattern of ~~said~~ the plurality of recesses; and

spreading ~~said~~ the nonsolid conductive material over ~~said~~ the stencil and into ~~said~~ the plurality of recesses with ~~a spread~~ spreading member.

14. (Currently Amended) The method of claim 12, further comprising inserting each of ~~said~~ the conductive bumps in a recess of ~~said~~ the plurality of recesses in contact with ~~said~~ the nonsolid conductive material therein.

15. (Currently Amended) The method of claim 14, further comprising bonding each of ~~said~~ the conductive bumps inserted in ~~said~~ the plurality of recesses to ~~said~~ the plurality of conductive elements using ~~said~~ the nonsolid conductive material.

16. (Currently Amended) The method of claim 1, wherein ~~said~~ providing ~~said~~ the wafer scale interposer substrate comprises providing ~~said~~ the wafer scale interposer substrate with at least one opening in ~~said~~ the first surface thereof at a location of each interposer substrate and placing and configuring ~~said~~ the at least one opening to communicate with at least one recess of ~~said~~ the plurality of recesses.

17. (Currently Amended) The method of claim 16, further comprising introducing dielectric filler material through ~~said~~ the at least one opening into a space adjacent ~~said~~ the conductive bumps in ~~said~~ the at least one recess.

18. (Currently Amended) The method of claim 1, further comprising introducing dielectric filler material into a space adjacent at least some of ~~said~~ the conductive bumps disposed in ~~said~~ the plurality of recesses.

19. (Currently Amended) The method of claim 1, wherein ~~said~~ providing ~~said~~ the wafer comprises providing a layer of encapsulation material on ~~said~~ the back surface ~~thereof~~ thereof.

20. (Currently Amended) The method of claim 19, wherein ~~said~~ providing ~~said~~ the layer of ~~said~~ the encapsulation material is effected by at least one of spin-coating and glob-top covering.

21. (Currently Amended) The method of claim 18, further comprising dicing ~~said~~ the wafer and ~~said~~ the wafer scale interposer substrate into singulated semiconductor device assemblies, each of ~~said~~ the singulated semiconductor device assemblies comprising at least one semiconductor die of ~~said~~ the plurality of semiconductor dice secured to at least one interposer substrate of ~~said~~ the plurality of interposer substrates.

22. (Currently Amended) The method of claim 21, further comprising at least partially encapsulating ~~said~~ the singulated semiconductor device assemblies by dispensing encapsulation material about a periphery of ~~said~~ the at least one semiconductor die of each of ~~said~~ the singulated semiconductor device assemblies.

23. (Currently Amended) The method of claim 1, further comprising dicing ~~said~~ the wafer disposed to ~~said~~ the wafer scale interposer substrate into singulated semiconductor device assemblies, each of ~~said~~ the singulated semiconductor assemblies comprising at least one semiconductor die of ~~said~~ the plurality of semiconductor dice secured to at least one interposer substrate of ~~said~~ the plurality of interposer substrates.

24. (Currently Amended) The method of claim 23, further comprising at least partially encapsulating ~~said~~ the singulated semiconductor assemblies by dispensing encapsulation material about a periphery of ~~said~~ the at least one semiconductor die of each of ~~said~~ the singulated semiconductor device assemblies.

25. (Currently Amended) The method of claim 24, wherein ~~said~~ the at least partially encapsulating ~~said~~ the singulated semiconductor device assembles comprises leaving ~~said~~ the back surface of ~~said~~ the at least one semiconductor die exposed.